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**CLASS : S.E. COMP SUBJECT : DEL**

**EXPT. NO. : 6 DATE : 13/12/2021**

**TITLE : RIPPLE COUNTER CIRCUIT**

**OBJECTIVE :**

1. Design and Implement 3-bit Asynchronous (Ripple) UP Counter circuit using IC-

74LS76

Draw Timing Diagram.

1. Design and Implement 3-bit Asynchronous (Ripple) DOWN Counter circuit using

IC-74LS76

Draw Timing Diagram.

1. Design and Implement MOD-N Asynchronous (Ripple ) UP Counter circuit using IC-

74LS76

Draw Timing Diagram.

**APPARATUS :**

Digital-Board, GP-4 Patch-Cords, IC-74LS76, IC-74LS32, IC-74LS04/IC-74LS08 and Required Logic gates if any

**THEORY :**

Counter is a Sequential Logic device which can be use to count the number of pulses given to the circuit. Counter can be classified into two category one is Synchronous and other is Asynchronous (Ripple) In case of Asynchronous counter output of first flip-flop goes to the clock of next and so on, and input of all flip-flop is connected to VCC for IC74LS76.

All set and reset pin is connected to VCC.Asynchronous counter is easy to design as compared to Synchronous Counter. Synchronous Counter is faster than Asynchronous Counter.IC-74LS76 is Dual M/S-JK filp-flop, which means in one IC there are two M/S-JK filp-flop are contained.

**PIN Diagram :**

PRESET1

PRESET2

CLOCK1

CLEAR1

CLEAR2

1

K

J

2

1

Q

1

Q

GND

K

2

Q

2

Q

2

CLOCK2

J

1

VCC

7

4

LS

7

6

D

U

A

L

MS

J-K

FF

**PROCEDURE :**

1. Make the connections as per the Logic circuit of 3-bit Ripple UP Counter circuit using IC74LS76 and Verify its Truth Table.
2. Make the connections as per the Logic circuit of 3-bit Ripple DOWN Counter circuit using IC-74LS76 and Verify its Truth Table.
3. Make the connections as per the Logic circuit of MOD-N Ripple UP Counter circuit using IC-74LS76 and Verify its Truth Table.

**Design of 3- bit Asynchronous UP- Counter**

**Logic Diagram:**

|  |
| --- |
|  |

**Observation Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLOCK PULSE** |  | **Output** |  |
| **QA** | **QB** | **QC** |
| **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** |
| **2** | **0** | **1** | **0** |
| **3** | **0** | **1** | **1** |
| **4** | **1** | **0** | **0** |
| **5** | **1** | **0** | **1** |
| **6** | **1** | **1** | **0** |
| **7** | **1** | **1** | **1** |

**Design of 3- bit Asynchronous DOWN- Counter**

**Logic Diagram:**

|  |
| --- |
|  |

**Observation Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLOCK PULSE** |  | **Output** |  |
| **QA** | **QB** | **QC** |
| **0** | **1** | **1** | **1** |
| **1** | **1** | **1** | **0** |
| **2** | **1** | **0** | **1** |
| **3** | **1** | **0** | **0** |
| **4** | **0** | **1** | **1** |
| **5** | **0** | **1** | **0** |
| **6** | **0** | **0** | **1** |
| **7** | **0** | **0** | **0** |

**Design of ( MOD - N = MOD-5 )Asynchronous DOWN-Counter**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Dec.Equ.** | **OUTPUT** | |  | **RESET**  **LOGIC** | | **QC** | **QB** | **QA** | **Y** | | 7 | **1** | **1** | **1** | **1** | | **6** | **1** | **1** | **0** | **1** | | **5** | **1** | **0** | **1** | **1** | | **4** | **1** | **0** | **0** | **1** | | **3** | **0** | **1** | **1** | **1** | | **2** | **0** | **1** | **0** | **0** | | **1** | **0** | **0** | **1** | **0** | | **0** | **0** | **0** | **0** | **0** |                             **K-MAP for RESET LOGIC:** |

**Logic Diagram:**

|  |
| --- |
|  |

**CONCLUSION:**

Hence, we have successfully implemented 3-bit up and down counter and MOD-5 ripple counter.

**REFFRENCE:**

1. **R.P.Jain “Modern Digital Electronics” TMH 4th Edition**

1. **D.Leach,Malvino,Saha,”Digital Principles and Applications”,TMH**

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